Analysis and Implementation of an Ultra-Wide Tuning Range CMOS Ring-VCO With Inductor Peaking

Ke Li, Fanfan Meng, Dave J. Thomson, Peter Wilson, and Graham. T. Reed

***Abstract*— A novel ring voltage controlled oscillator (VCO) topology is proposed which uses monolithic inductors as a peaking load. Four design examples have been fabricated and tested to verify the proposed circuit structure. The highest measured oscillation frequency is 25.07 GHz, with a tuning range of more than four octaves, and the active area is 0.0085 mm^2. The design has the highest combined frequency and tuning range with the best figure of merit (≈ 195) comparable to previously published work.**

***Index Terms*— Delay cell, inductor peaking, ring oscillator, VCO.**

I. Introduction

AS DATA traffic continually increases, the date rate in wireline transceivers has exceeded 25Gb/s [1]. Traditionally, all the clock generation systems [Phase-Locked Loop (PLL) and Clock Data Recovery (CDR)] in these transceivers are based on LC (Inductor-Capacitor) tank VCOs. The main reason for this is that LC-VCOs have inherently excellent phase noise performance and usually a relatively high oscillation frequency, which make them appropriate for wireless and optical transceivers [2], [4]. However, one significant drawback with LC-VCOs is that they have a relatively small tuning range, potentially reducing the data-rate range that a transceiver can operate at. In contrast to the LC based Oscillators, Ring Oscillator (RO) based VCOs are attractive for digital applications and copper based wireline transceivers owing to their wider tuning range, ease of integration and small die area [2].

Although LC-VCOs and RO-VCOs are considered as opposite solutions due to the seemingly opposing features described previously, it is possible to take an innovative approach to combine the advantages of these two methods. This approach is inspired by previous work [3], which adopting several monolithic inductors with three stages of ring oscillator to achieve a terahertz frequency. In this work we therefore focus on an implementation of incorporating peaking inductors with a typical RO-VCO structure, to obtain a combination of ultra-wide tuning range and small die area. To demonstrate the functionality and advantages of the proposed circuit topology, four RO-VCO designs have been implemented using the 130 nm and 65 nm processes. As shown later in this letter, the VCO implemented on the 65 nm process can operate up to 25.07 GHz with a tuning range of more than four octaves. The theoretical analysis of proposed RLC-RO-VCO is presented in section II. Four design examples are then presented in section III, associated with measurement results of each example. Finally, section IV concludes the letter.

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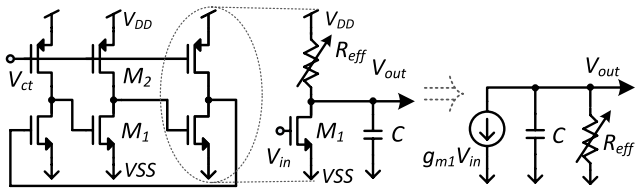

Fig. 1. Common source amplifier based RO-VCO.

II. Theoretical analysis

It is well-known that any RO must satisfy two of Barkhausen's criteria for oscillation, namely, the phase shift around the total feedback loop must be a multiple of 360° at its oscillation frequency and the magnitude of the loop gain at that frequency must be unity [4].

Therefore for a typical three stage RO-VCO as shown in Fig. 1, each delay cell can be treated as a common source amplifier, with its transfer function given as:

$$H(s) = V_{out}/V_{in} = -g_{m1}R_{eff}/(1 + sCR_{eff}) \qquad (1)$$

The capacitance C denotes all the capacitance associated at the V_{out} node, and a variable resistor R_{eff} is used to represent the effective resistance of the transistor M2, whose gate voltage is controlled by the external signal V_{ct}. From (1), it can be seen that 3-dB bandwidth of this amplifier is $1/(2\pi R_{eff}C)$, and frequency tuning is realized by changing the effective resistance R_{eff} of transistor M2. In addition to the variable resistance R_{eff}, the gate capacitance C in the load stage and the parasitic capacitance associated with wiring limit the maximum achievable frequency.

In order to enhance the achievable bandwidth of the amplifier in spite of these capacitances, an optimally valued inductor can be inserted to provide a resonant circuit with this capacitance. This technique, known as inductor peaking, is a fundamental technique that is commonly adopted for high-speed amplifier design [4]. As shown in Fig. 2, a typical RO-VCO can be modified by inserting an additional inductor L within

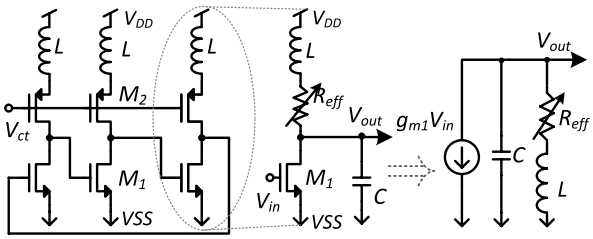

Fig. 2. Addition of peaking-inductor with RO-VCO.

TABLE I
PARAMETERS OF FOUR DESIGN EXAMPLES

	IBM 130nm 8RF CMOS		TSMC 65nm LP CMOS	
	VCO-1	**VCO-2**	**VCO-3**	**VCO-4**
VDD(V)	1.5	1.5	1.2	1.2
M1(W/L) (μm)	22.5/0.12	22.5/0.12	20/0.06	20/0.06
M2(W/L) (μm)	72/0.12	72/0.12	64/0.06	64/0.06
Inductance (pH)	**≈590**	**≈420**	**≈350**	**≈350**
Peak Q@GHz	**18.3@12**	**7.2@34**	**21.5@26**	**12.5@33**

each delay cell, with the resulting transfer function given in (2):

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}(R_{eff} + sL)}{s^2CL + sCR_{eff} + 1} \tag{2}$$

Re-organizing (2) gives (3)

$$\frac{V_{out}}{V_{in}} = -g_{m1}R_{eff}\frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{\omega_n}{2\zeta} \tag{3}$$

Where the nature frequency ω_n and damping factor ζ are given by (4)

$$\omega_n = 1/\sqrt{LC}; \zeta = (R_{eff}/2) \cdot \sqrt{C/L} \tag{4}$$

It is interesting to note that (4) reveals two important facts that can guide the design of inductor-peaked RO-VCOs. First, for a fixed damping factor ζ, the inductance L is proportional to the capacitance C. Thus for an advanced CMOS process node which has smaller gate capacitance, the required peaking inductance could be reduced proportionally, which results in smaller silicon area with a more compact design. Secondly, for a given design, the smallest (worst) damping factor ζ occurs at the lowest value of R_{eff}, which is also the point at which the VCOs operate at their highest frequency. Therefore, decreasing the frequency (frequency-tuning mechanism) has little negative effect on the loop stability. Furthermore, for practical implementation of on-chip monolithic inductors, there is usually a concern about the trade-off between the quality factor (Q) of the inductor and the physical inductor size. We show later in this letter that the size of the inductor may influence the frequency range, whereas the Q may dominate the phase noise performance of proposed RO-VCO.

III. EXPERIMENTAL RESULTS

To validate the proposed design approach, four design examples were fabricated at two different process nodes with the key parameters listed in Table I.

The key difference is the inductors realized in VCO-1/3 only use the top ultra-thick metal layer whereas the inductors realized on VCO-2/4 use stacked inductor structure on inner thinner layer, which results in a lower quality factor (Q)

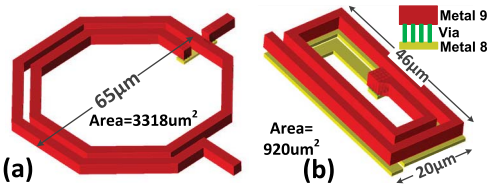

Fig. 3. Layout view of the inductors used with VCO-3(a) and VCO-4(b).

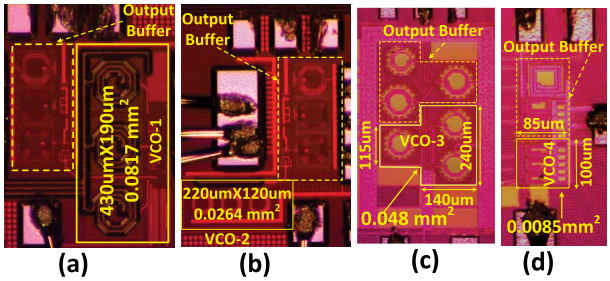

Fig. 4. Micoscope view of the proposed four RO-VCO designs.

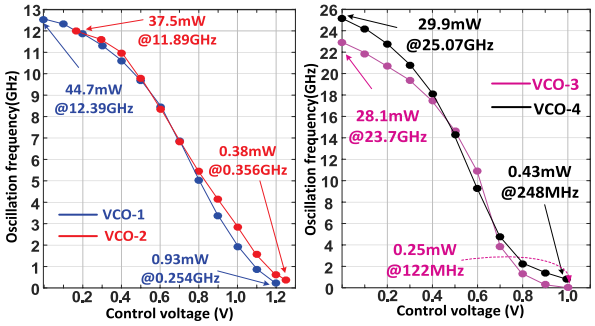

Fig. 5. Measured frequency tuning characteristics.

and a smaller silicon area. As illustrated in Fig. 3, the stacked inductor occupies less than one-third of silicon area compared to the inductor used with VCO-3, although the cost in performance is a relatively lower Q factor. Micrographs of the four design examples are shown in Fig. 4. It can be seen that the VCOs realized in the 65 nm process node have much smaller silicon area than the corresponding designs realized in 130 nm process node. This is consistent with the theoretical prediction that the value of peaking inductor should be smaller in the advanced process node.

The output RF signal from each design example was fed into Keysight E4446A spectrum analyser. In summary, the measured voltage-frequency tuning characteristics of each design example are shown in Fig. 5, with the power consumption highlighted at the extremes of the tuning range. With the premise that identical transistor sizes were used in each pair of design examples, it is reasonable that they should have similar frequency-voltage tuning range characteristics. However, as highlighted in Fig. 6, there is a considerable difference when comparing the highest oscillation frequency of VCO-3 and VCO-4. The reason is that the large inductors used with VCO-3 indeed extend the signal wiring between each delay cell, which itself introduces a considerable additional parasitic capacitance, while the stacked-inductors used with VCO-4 eliminate this issue. This implies that using a stacked-inductor not only reduces the overall silicon area, but can also

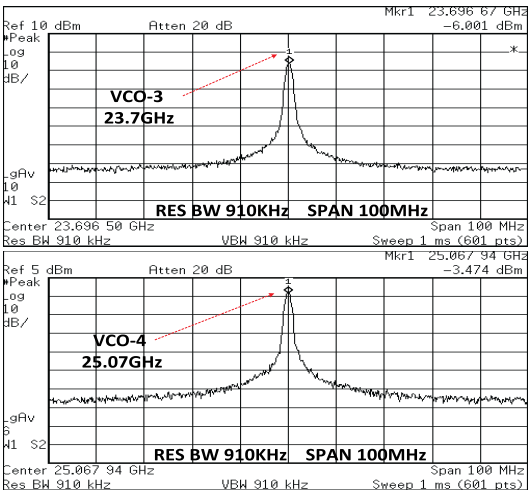

Fig. 6. The spectrum of highest oscillation frequency of VCO-3/4.

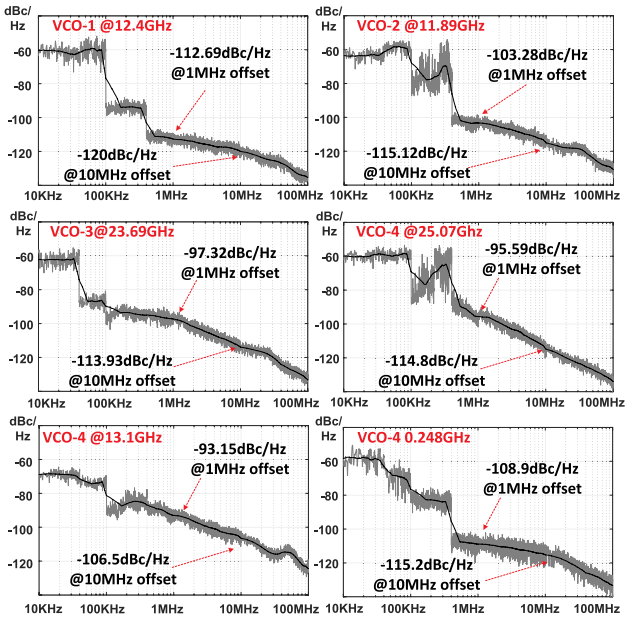

Fig. 7. Measured phase noise results of each design example.

benefit the tuning range of the proposed VCO by having an intrinsically lower parasitic capacitance.

As shown in Fig. 7, the measured phase noise results of each design example at its highest oscillation frequency are plotted. In additional to this, the phase noise performances of VCO-4 at its middle and lowest oscillations frequency are provided. Although a battery based power supply system is used to provide a clean power source, some environmental interference still can be observed at several hundred KHz; but this does not prevent two conclusions can be obtained from these measurement figures. First, when tunning the oscillation frequency, phase noise performance does get slightly worse in the middle range, which was suppose due to the fact that inductor has smaller quality factor (Q) at this lower frequency range. Secondly, it can be observed that both VCO-1/3 (big size) show better phase noise performance than their counterpart

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[5]	[6]	[7]	VCO-2	VCO-4
Process	65nm	130nm	180nm	130nm	65nm
FTR range (Hz)	120% 2G-8G	161% 1G-9.4G	25.6% 10G-13.5G	189% 0.36G-11.9G	196% 0.25G-25G
PDC(mW)	6.4	3.7	2.4	37.5	29.9
PN dBc/Hz@ f_{off}/f_{osc} (Hz)	-101@ 1M /4.2G	-112@ 10M /6G	-104.5@ 1M /12.7G	-103.3@ 1M /11.89G	-95.6@ 1M /25.07G
FOM	187	186	188.2	**195.3**	**194.7**

VCO-2/4 (small size), which is supposed due to the fact that inductors used in VCO 1/3 have higher quality factor than the inductors used in VCO-2/4. However, as illustrated in Table II, based on the normally used Figure of Merit (5) [5], these two small VCOs still demonstrate a considerable better performance when compared with the recent published results, provided that the smallest design only occupy 0.0085mm^2 silicon area

$$FOM = -PN(f_{off}) + 20\log\frac{f_{osc}}{f_{off}} - 10\log\frac{P_{DC}}{1mW} + 20\log\frac{FTR}{10} \quad (5)$$

IV. CONCLUSION

In this letter, we have demonstrated the feasibility of incorporating peaking inductors in Ring Oscillator VCOs. Experimental results show that the proposed circuit topology can take advantage of modern deep sub-micron processes, which may be used for clock generation and other similar applications in future advanced systems. The results indicate the best figure of merit ($\approx$ 195) in the field and the best combination of frequency and tuning range to the authors' knowledge. We would suggest that useful future work would be to use the symmetrical inductor with differential delay cells, and embed it in a PLL design.

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